



Queen Mary

University of London

Science and Engineering

Radiation Detectors (SPA 6309)

Lecture 8

Peter Hobson

What is this lecture about?

- The principles of detection of ionising radiation
 - Interaction of charged and neutral particles with matter
 - Gaseous sensors
 - **Semiconductor sensors**
 - Scintillators
- Sensor systems used in particle and nuclear physics
 - Calorimeters
 - Tracking detectors
 - Neutrino detectors

Key points from previous lecture

- Semiconductor sensors have replaced gas-based sensors in almost every particle tracking application (except TPC)
- Scale of silicon sensor systems has expanded from $< 0.1 \text{ m}^2$ silicon (1980s) to 200 m^2 (CMS tracker at LHC).
- e/h pairs separated by external reverse bias in the *depletion* region
- Signal comes from electrons and holes moving under an external electric field.
- XY readout possible from a single silicon plane using p on n and n⁺ on n strips on opposite sides
- Sensors are intrinsically fast due to small distance over which e/h move plus high mobilities.

Acknowledgements

- Figures/text from a number of sources.
 - F. Hartmann *Nuclear Instruments and Methods in Physics Research A* **666** (2012) 25–46 F
 - W. Snoeys *Nuclear Inst. and Methods in Physics Research A* **938** (2019) 41–50
 - P. Allport *Nature Reviews: Physics* **1** (2019) 567-576
 - C. Da Via et al, *Nuclear Inst. and Methods in Physics Research A* **694** (2012) 321–330
 - D.M.S. Sultan et al, *JINST* **10** (2015) C12009

Revision!

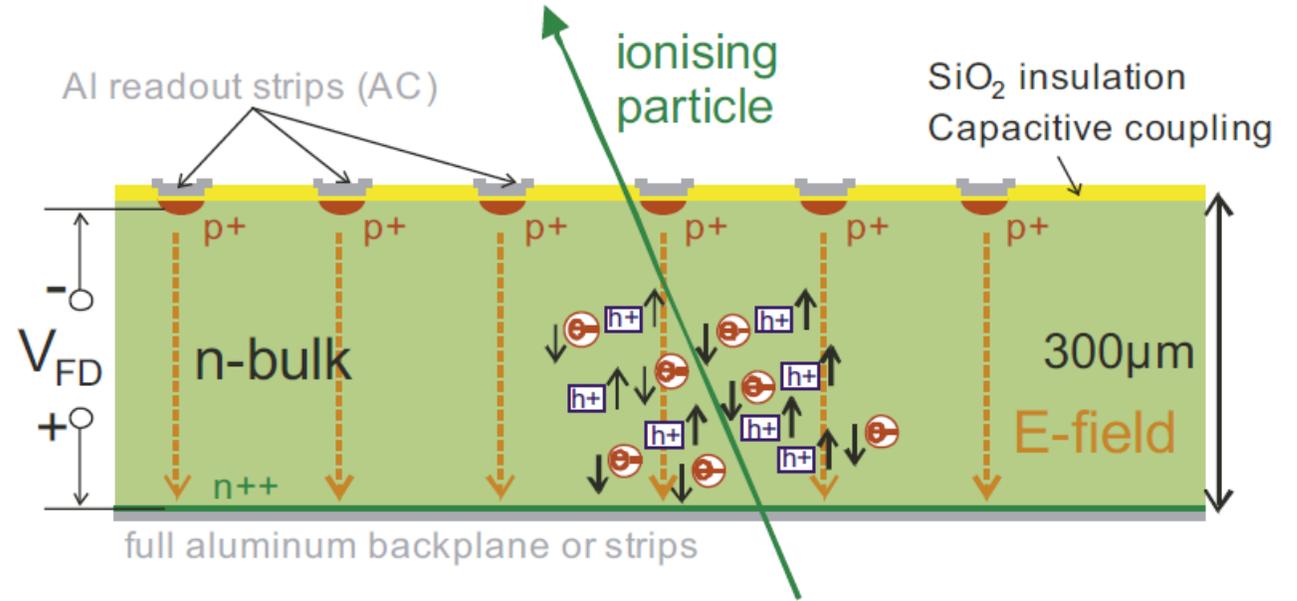
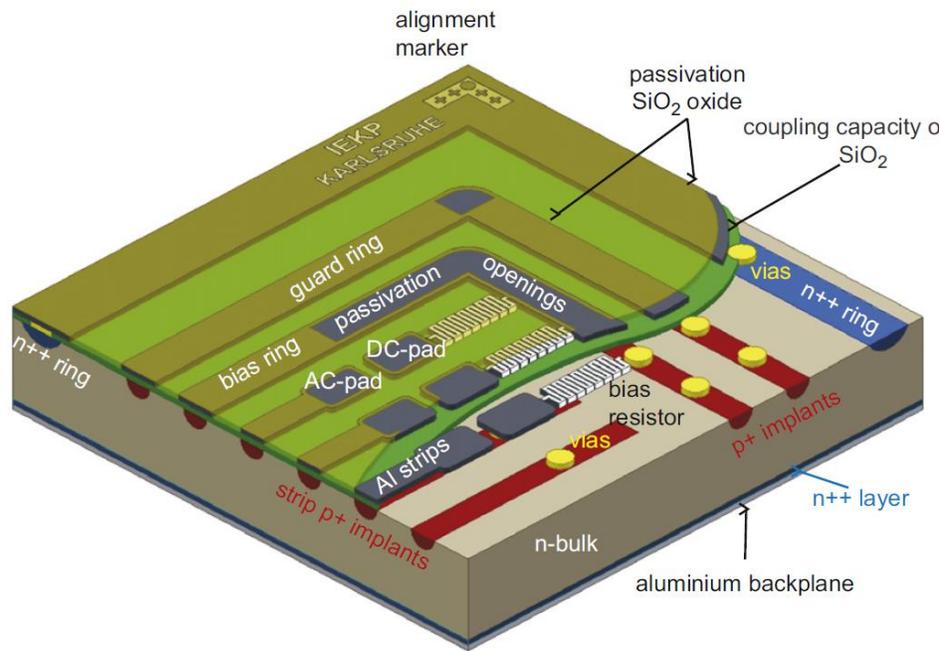


Fig. 2. Working Principle of an AC-coupled Silicon Micro-Strip Detector. Electron-hole pairs resulting from the ionization of the crossing charged particle, according to the Bethe-Bloch-formula, travel to the electrodes on the sensor planes. The segmentation into individual pn-junctions makes it possible to collect the charges on a small number of strips only, where they capacitively couple to the Al readout strips. The latter are connected to the readout electronics, where the intrinsic signal is shaped and amplified. In the case of segmented p strip implants in an n-bulk silicon material, holes are collected at the p strips.

Revision!

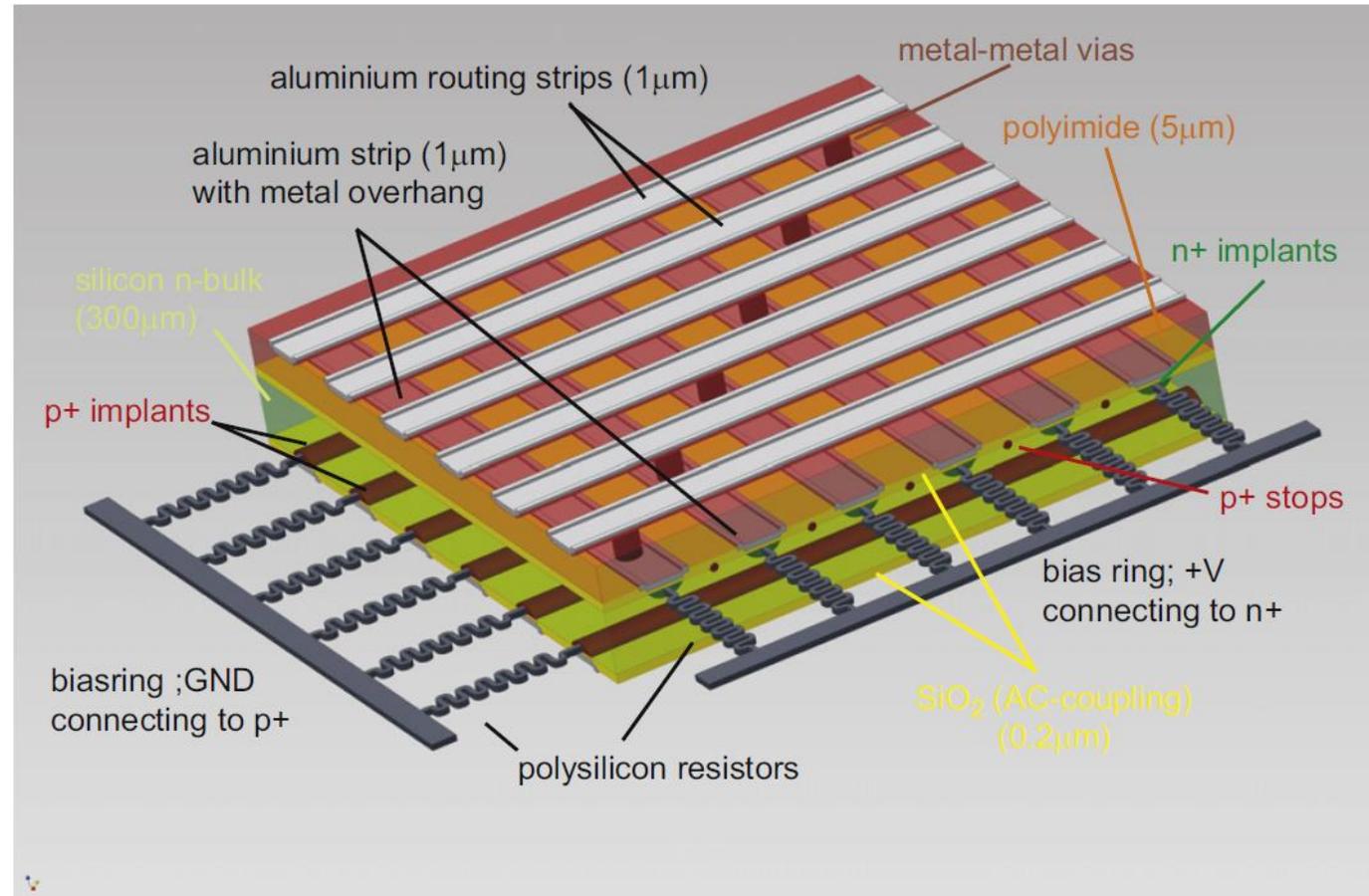


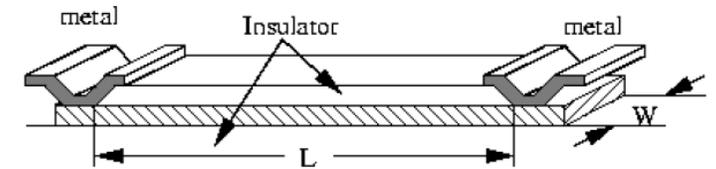
Fig. 5. The DELPHI double sided, double metal sensor scheme. The sensors contain novel integrated coupling capacitors. The bias is applied via highly resistive polysilicon resistors. The n-side strips are routed via a second metal routing layer, and the innovative field plate configuration guarantees 100 M Ω n strip isolation [5].

CMOS resistors

TYPES OF INTEGRATED RESISTORS

A resistor is made of a strip of resistive layer.

$$R = 2R_{\text{cont}} + \frac{L}{W} R_{\square}$$

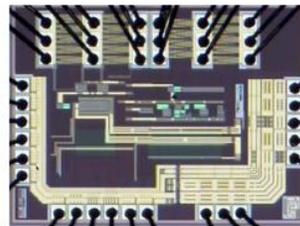


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The Laboratory research activities aims at different design targets. Generally speaking, research focuses on design, modeling and characterization of analog and mixed analog-digital systems for signal processing, using either pure CMOS or BiCMOS technology. More specifically, our research group is involved in the design of innovative solutions and architectures for: analog-to-digital (A/D) and digital-to-analog (D/A) converters; non-volatile memory storage (in particular Flash and Phase Change Memories); interfaces for sensors. Research programs are typically carried out in cooperation with international partners as semiconductor industries or Universities.

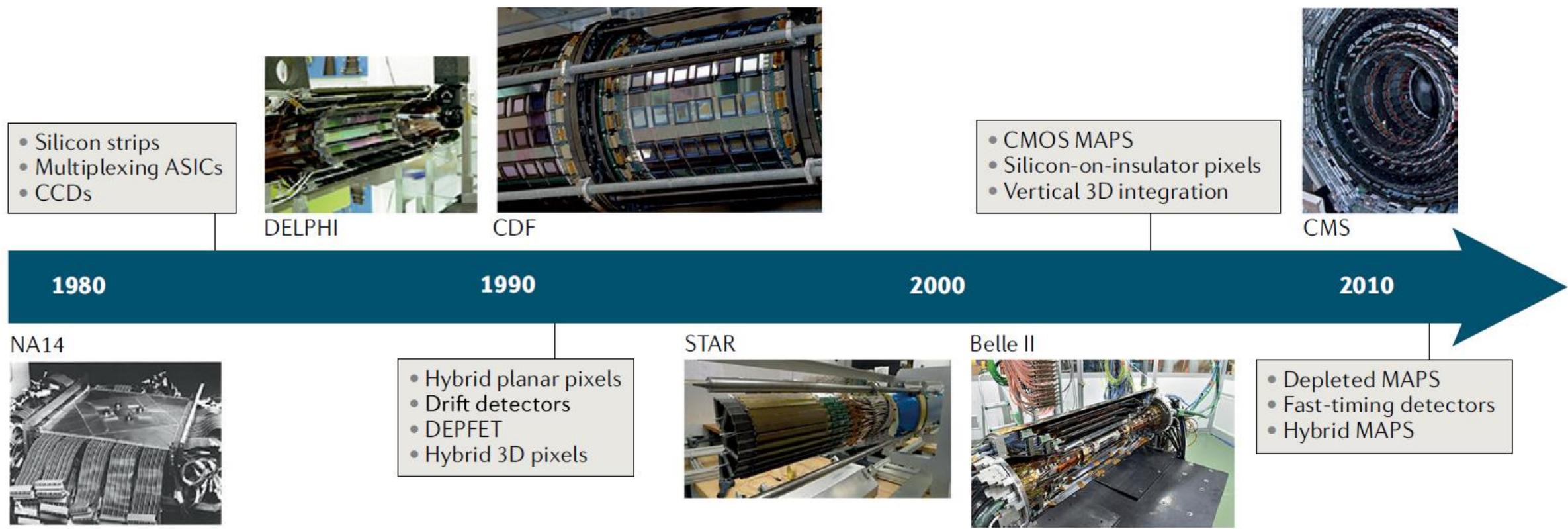
Research Areas:

- Integrated Circuits for Signal Processing
- A/D and D/A Converters
- Non-Volatile Memories
- Interface Circuits for Sensors
- DC-DC Integrated Circuits



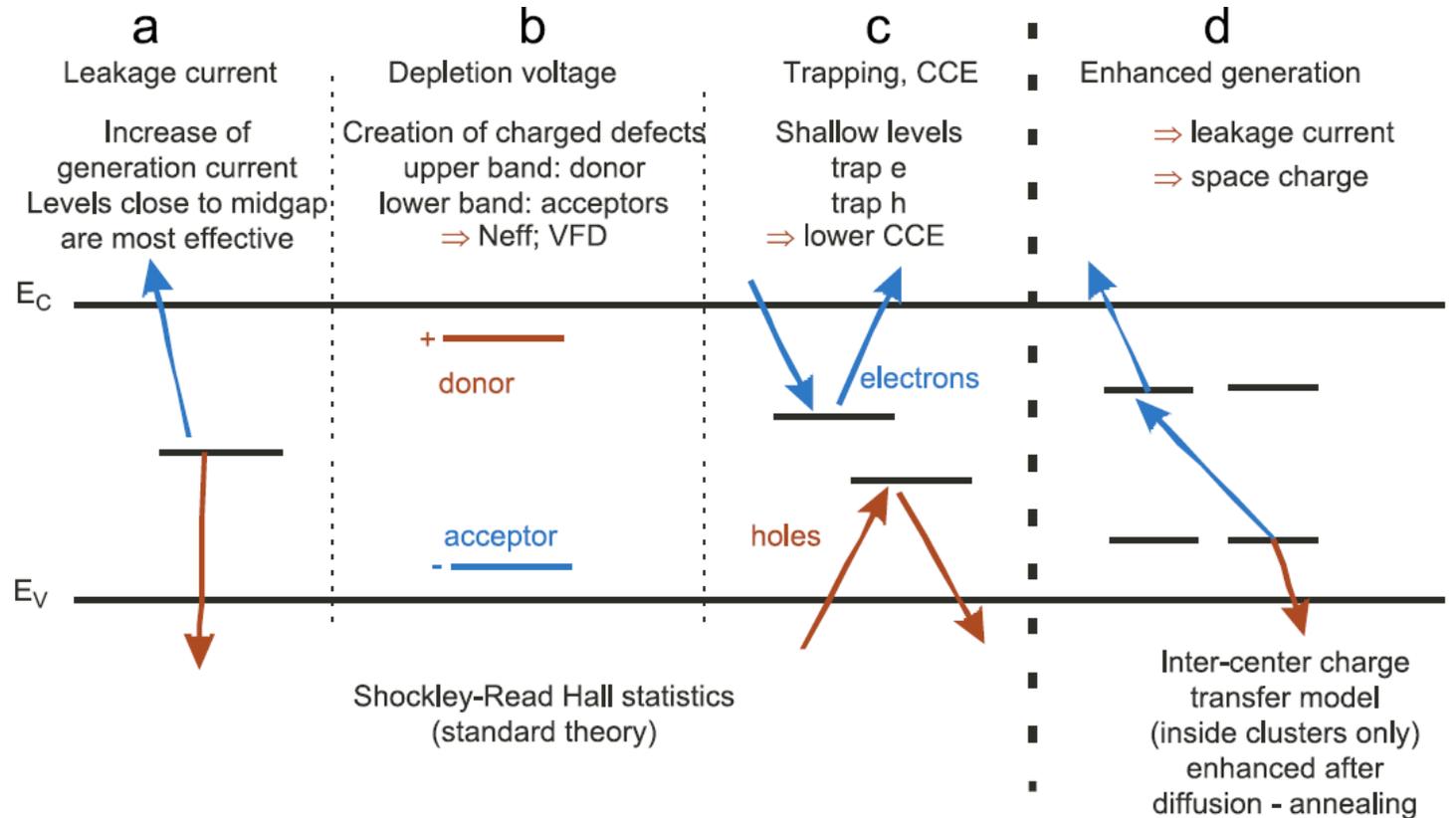
Type of layer	Sheet Resistance Ω/\square	Accuracy %	Temperature Coefficient ppm/ $^{\circ}\text{C}$	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 - 150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

Timeline

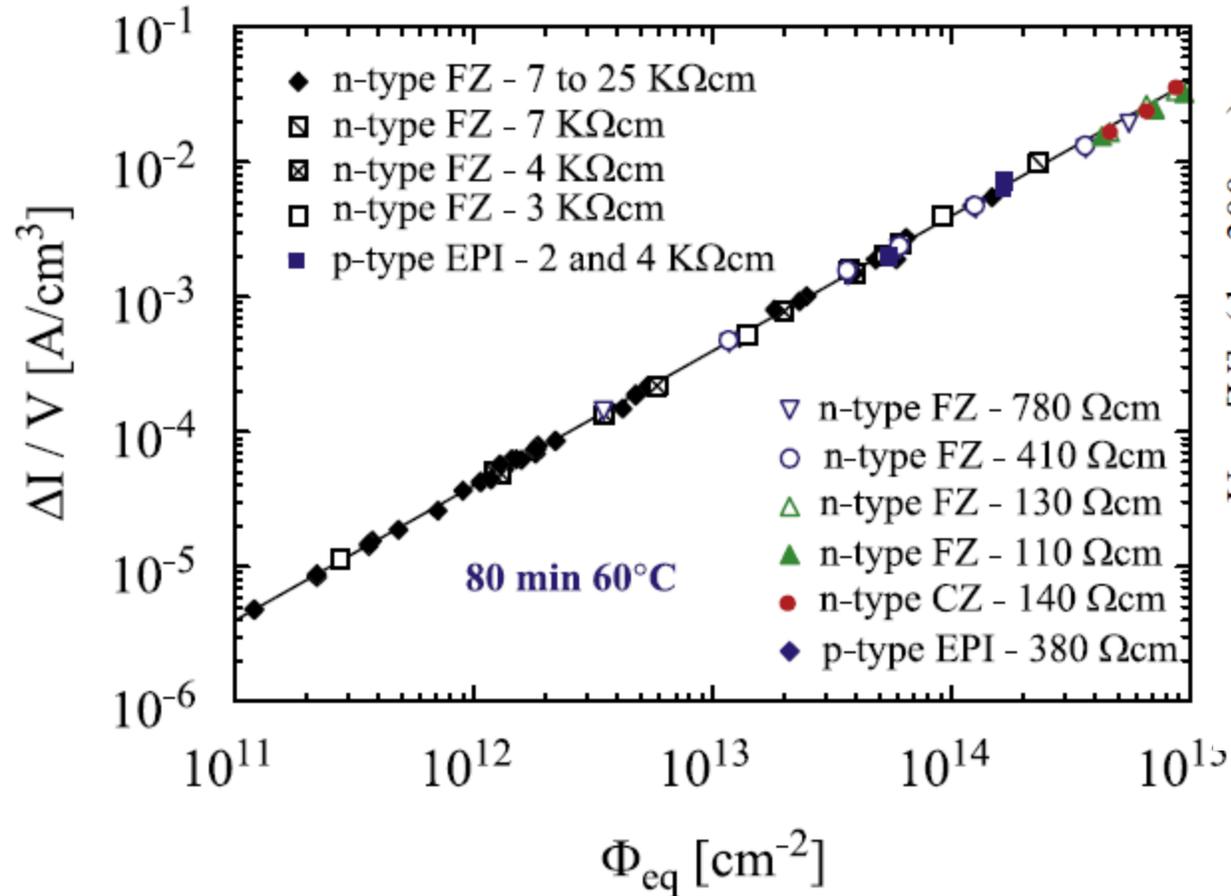


Radiation damage

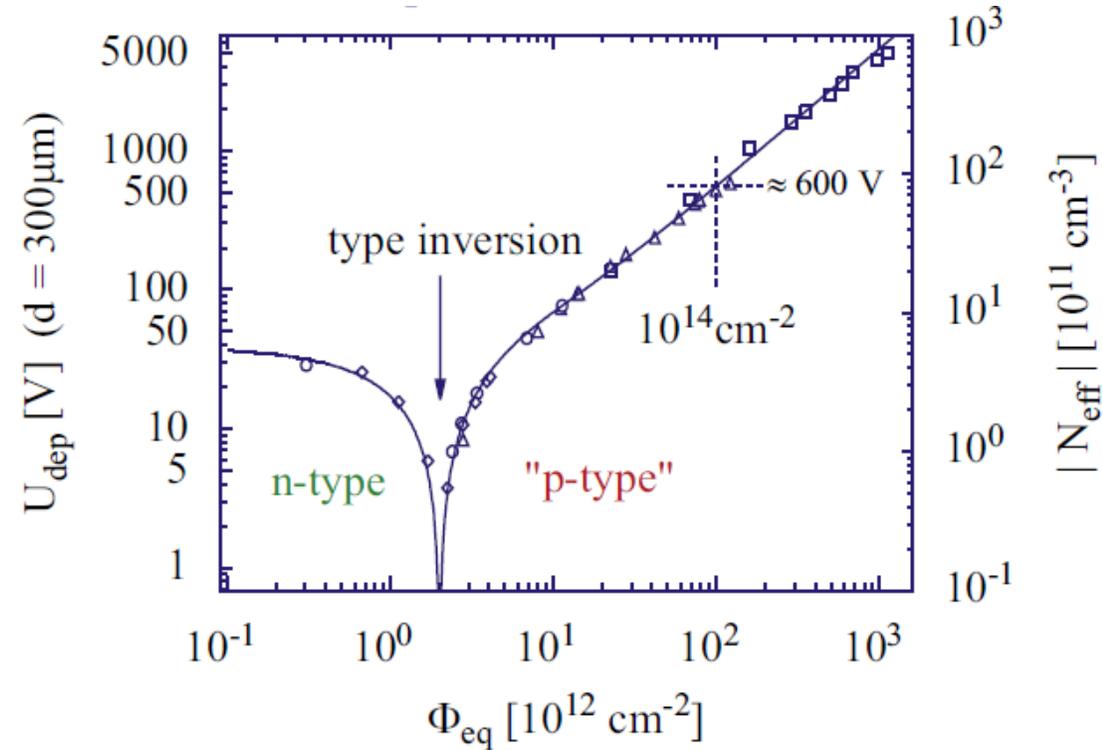
The different defect level locations and their effects. All relevant defect levels due to radiation are located in the forbidden energy gap. (a) Mid-gap levels are mainly responsible for dark current generation, according to the Shockley–Read–Hall statistics, and for decreasing the charge carrier lifetime of the material. (b) Donors in the upper half of the band gap and acceptors in the lower half can contribute to the effective space charge. (c) Deep levels, with trapping times larger than the detector electronics peaking time, are detrimental. Charge is “lost”; the signal decreases and the charge collection efficiency is degraded. Defects can trap electrons or holes. (d) The theory of the inter-center charge transfer model says that combinations of the different defects in defect clusters can additionally enhance the effects.



Radiation damage



Leakage current vs particle fluence



Depletion voltage vs particle fluence

Monolithic Active Pixel (MAPS)

Nikon Z7 camera

46 M pixel CMOS sensor (designed by Nikon, Sony Fab).



- Michael Kramer [CC BY-SA (<https://creativecommons.org/licenses/by-sa/3.0/>)]

MAPS concept

- Commercial CMOS optical sensor explosion (webcams, mobile phone, DSLR etc.)
- Build local electronics (amplifier, charge storage etc.) into *every single pixel* on a sensor chip (complete opposite to the charged coupled device CCD concept)
- Piggyback off the commercial processes to build fast radiation tolerant radiation sensors.

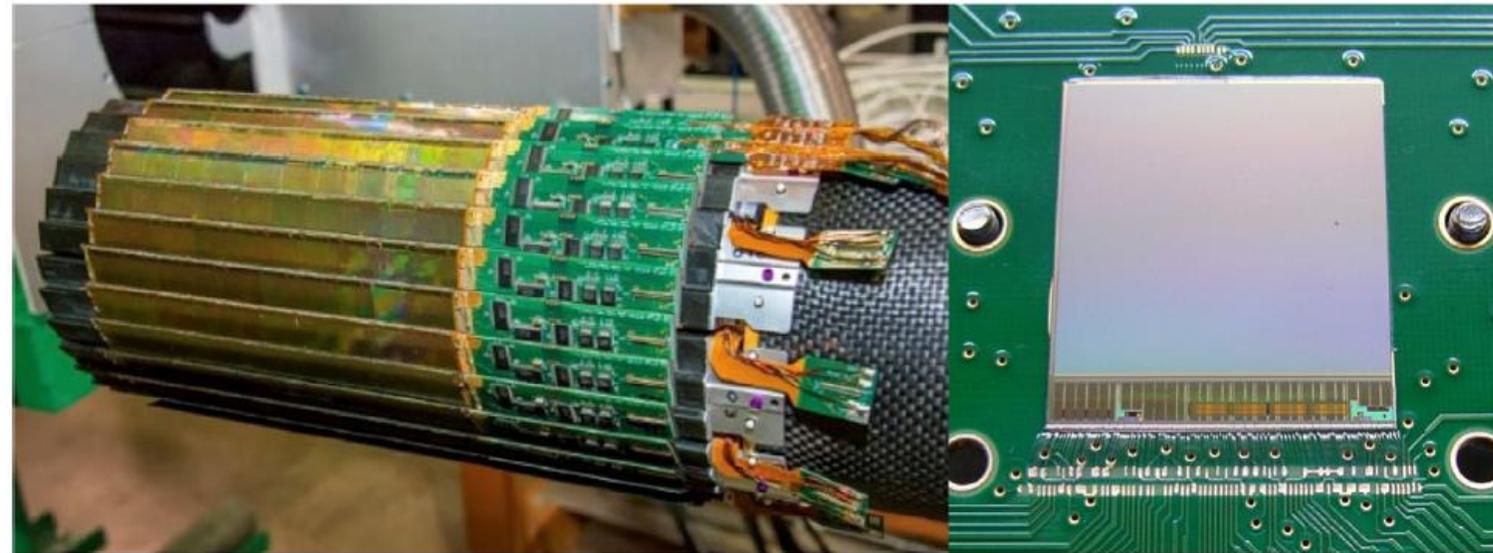
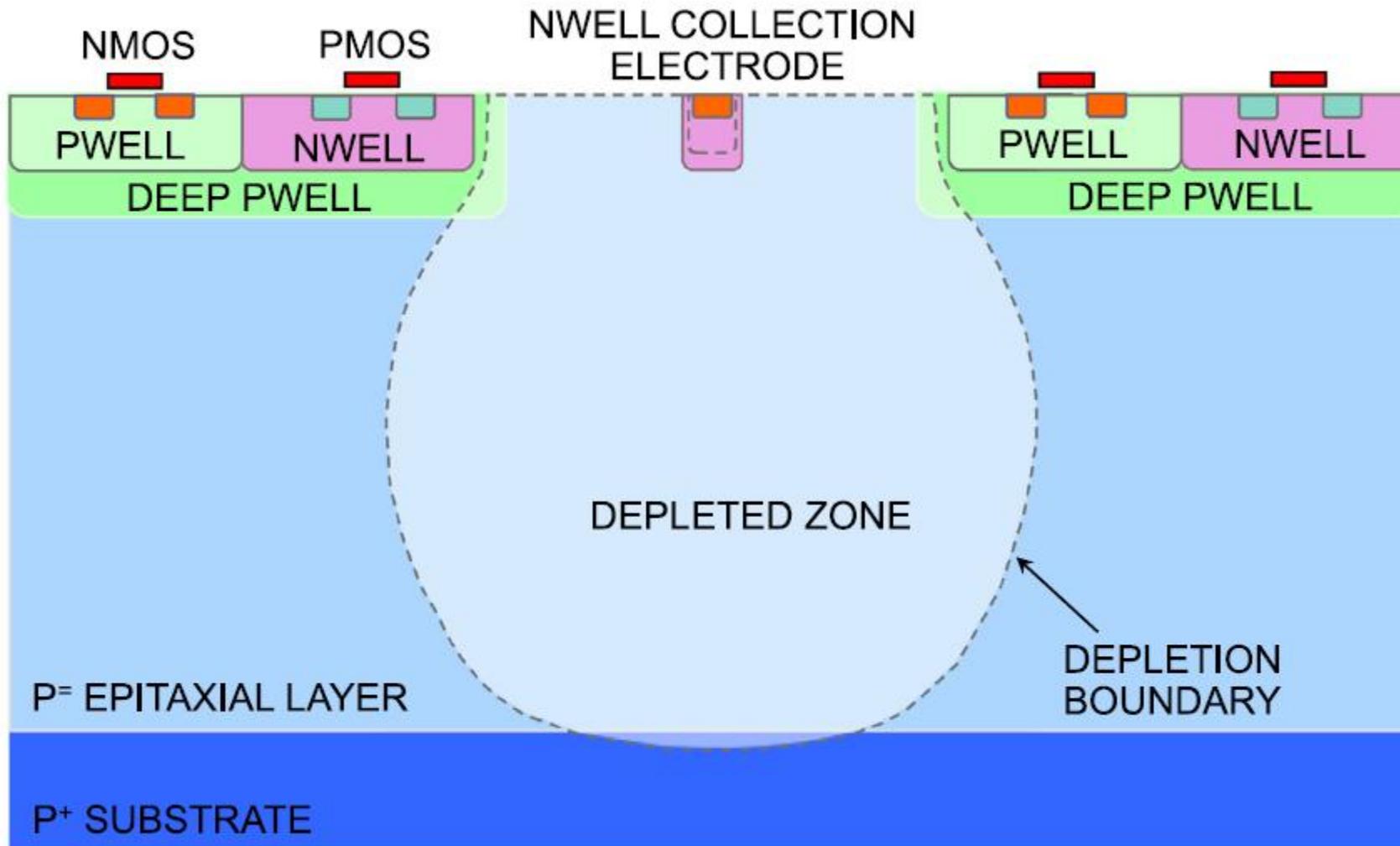
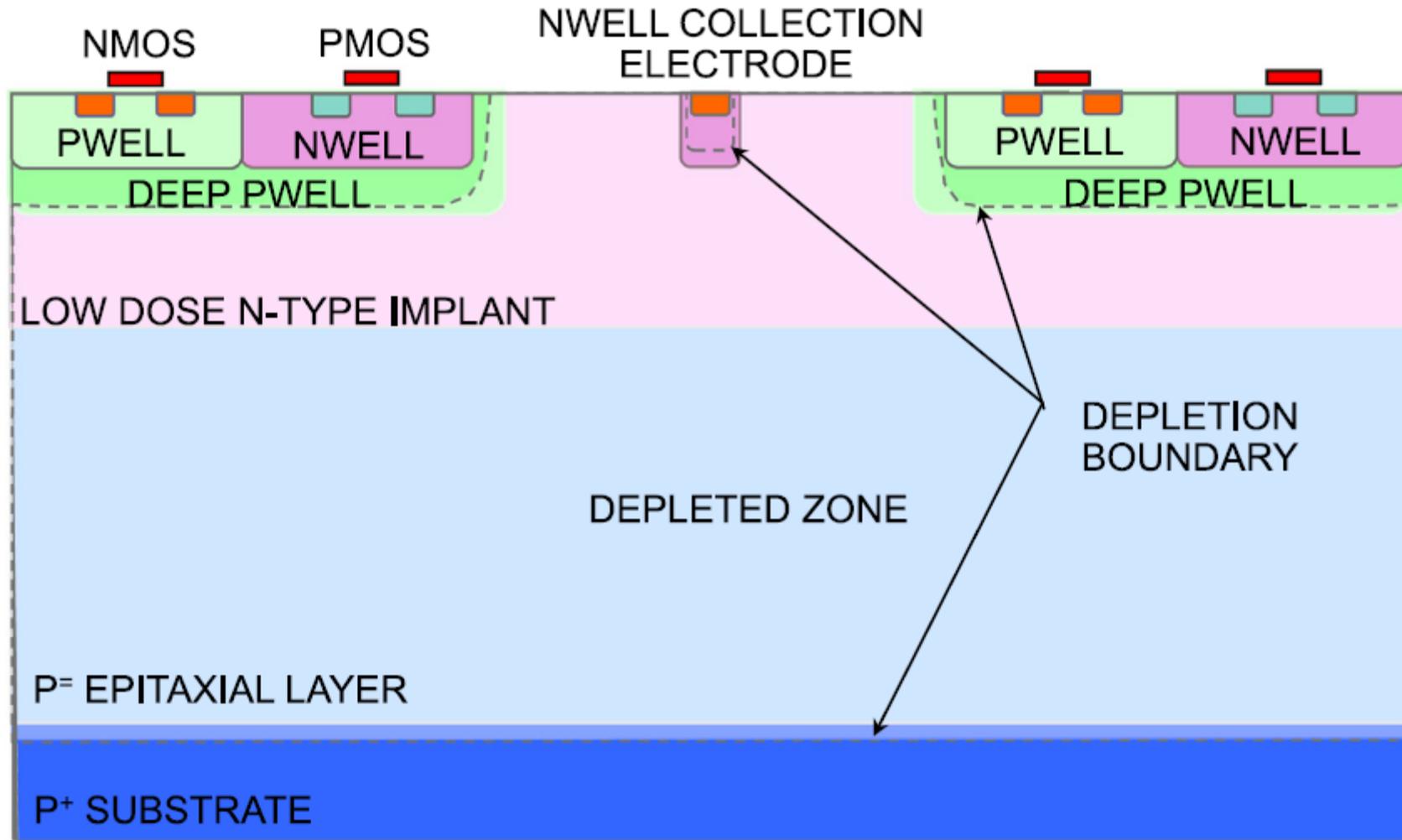


Fig. 1. The vertex detector of the STAR experiment [7], the first to use CMOS MAPS, and a die picture of the ULTIMATE CMOS sensor chip used for this detector

Tower Jazz standard imaging CMOS



Tower Jazz modified CMOS



Passive Sensors

Technology	Experiments	Advantages	Limitations
Strip detectors	<ul style="list-style-type: none"> • Fixed target (CERN): NA14, NA32, WA82, NOMAD-STAR, COMPASS • Fixed target (FNAL): E605, E653, E687, E771, E772, E789, E791 • $Sp\bar{p}S$: UA2 • SLC: Mark II • LEP: ALEPH, DELPHI, OPAL, L3 • Tevatron: CDF, D0 • c, b factories^a: BaBar, Belle, CLEO • HERA: H1, ZEUS, HERA-B, HERMES • LHC: ALICE, ATLAS, CMS, LHCb • RHIC: PHENIX, PHOBOS, STAR • LHCb Phase-I^b • LHC Phase-II Upgrades^b • ILC^c, LHeC^c, FCC^c 	<ul style="list-style-type: none"> • Simple, large-area fabrication and suitable for inexpensive interconnect technologies • Can be thinned but at the cost of less signal • Edge-only connections 	<ul style="list-style-type: none"> • Readout is either one or two (if double sided) projections • Capacitance seen by readout can be high • Bulk doping varies with radiation as does carrier lifetime
Planar pixel detectors	<ul style="list-style-type: none"> • WA97, DELPHI, NA62, ALICE, ATLAS, CMS, PHENIX • LHCb Phase-I^b, LHC Phase-II Upgrades^b • ILC^c, CLIC^c, FCC^c 	<ul style="list-style-type: none"> • True space-point information much better for congested tracks close to collision vertex • Low capacitance so low noise and therefore can be efficient at lower signals (such as for thinner sensors or after irradiation) 	<ul style="list-style-type: none"> • Flip-chip technologies are expensive • Both readout chip and detector need thinning to reduce multiple scattering • Depleted volume and charge trapping change with radiation damage to substrate
Three-dimensional pixel detectors	<ul style="list-style-type: none"> • ATLAS • LHC Phase-II Upgrades^b • FCC^c 	<ul style="list-style-type: none"> • Compared with planar pixel detectors, the required voltage to fully deplete the entire device both before and after irradiation is much lower • Required drift distances are less, giving excellent radiation hardness • No additional processing steps needed to achieve 'edgeless' detectors 	<ul style="list-style-type: none"> • The processing of doped columns through the substrate is costly and suitable vendors are limited • Larger capacitance between pixels than planar designs so thicker sensors needed for good signal/noise
Drift detectors	RHIC: STAR, ALICE	<ul style="list-style-type: none"> • Uses drift time to measure second coordinate in edge readout detector • Low capacitance 	<ul style="list-style-type: none"> • Drift time variation due to non-uniformity of substrate material • Trapping due to radiation

Active & Fast Timing Sensors

Technology	Experiments	Advantages	Limitations
Fast-timing detectors	<ul style="list-style-type: none">• LHC Upgrades^a• EIC^b, FCC^b	Few tens of picosecond timing capability in segmented detector with intrinsic gain	<ul style="list-style-type: none">• Gaps between multiplication layer implants inefficient so pitch cannot be too small• Current designs have issues with radiation hardness much beyond particle fluences of order 10^{15} cm^{-2}
Active sensors: DEPFET	Belle II	<ul style="list-style-type: none">• Very low noise readout possible• In-sensor data storage capability	<ul style="list-style-type: none">• Poor tolerance to radiation• Speed
Active sensors: CMOS hybrid pixels	FCC ^b	<ul style="list-style-type: none">• Retains the ability to employ low-cost CMOS imaging sensor technologies while still using advanced very fine feature size CMOS for digital electronics• Can multiplex several pixel outputs into one connection pad	Bump bonding can be reduced or avoided completely, but precision attachment and alignment still require expensive flip-chip techniques

Monolithic Sensors

Technology	Experiments	Advantages	Limitations
CCD and CCD-inspired detectors	NA32, SLD, ILC ^b , CLIC ^b	<ul style="list-style-type: none"> • Superb gain uniformity • Low noise, so signal region can be thin (better for angled tracks and allows back-thinning) • Mature commercial imaging technology • Very small pixel sizes possible 	<ul style="list-style-type: none"> • Slow readout • Low tolerance to both ionizing and bulk radiation damage
Silicon-on-insulator detectors	ILC ^b	<ul style="list-style-type: none"> • Mature technology • Separation of electronics and sensor substrates while still providing monolithic sensor • Excellent isolation of transistors reducing parasitic effects allowing lower power operation • Through-silicon-via technology gives added flexibility in array design 	<ul style="list-style-type: none"> • Complicated processing with many steps liable to affect yield • Many oxide interfaces that can trap charge produced by ionizing radiation
Small fill factor MAPS	<ul style="list-style-type: none"> • STAR • ALICE^a • ATLAS^b • LHCb^b, ILC^b, CLIC^b, EIC^b, LHeC^b, FCC^b 	<ul style="list-style-type: none"> • CMOS imaging sensor technology in widespread use • Small signal collection nodes separate from the deep p-well containing electronics offer low capacitance and hence lower noise such that the signal region can be thin (as for CCDs) • Low voltages adequate for good signal/noise • Fast charge collection 	Difficult to collect charge from under electronics unless additional substrate processing is used, which moves the diode junction to within the substrate rather than at the signal-collecting node
Large fill factor MAPS	<ul style="list-style-type: none"> • Mu3e^a • ATLAS^b • LHCb^b, ILC^b, CLIC^b, EIC^b, LHeC^b, FCC^b 	<ul style="list-style-type: none"> • Suitable HV-CMOS processing available from multiple vendors • Charge collection by deep n-well containing the pixel circuitry • Full charge collection • Possible to deplete to large depth giving large signal 	<ul style="list-style-type: none"> • Larger capacitance giving larger noise and slower rise time • Substrate doping and depletion depth change with dose owing to bulk damage • Deeper depletion gives greater charge spread for angled tracks

3D concept

- Decouple the active thickness Δ (and thus signal size due to ionisation) from the charge collection distance L .

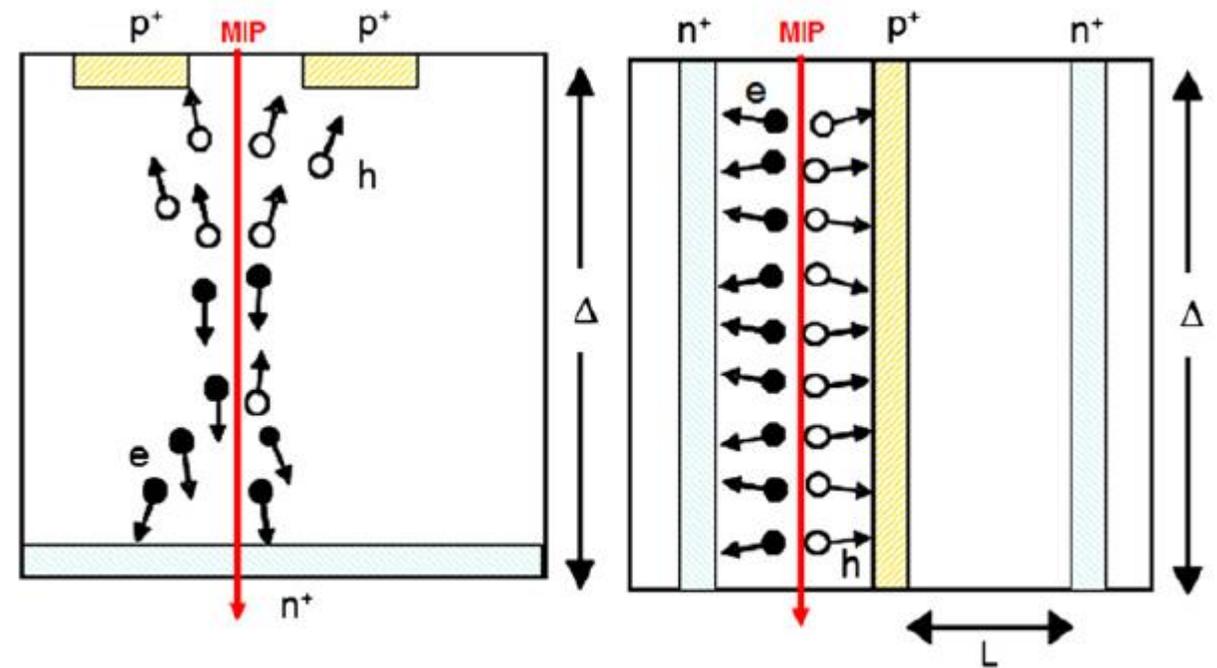
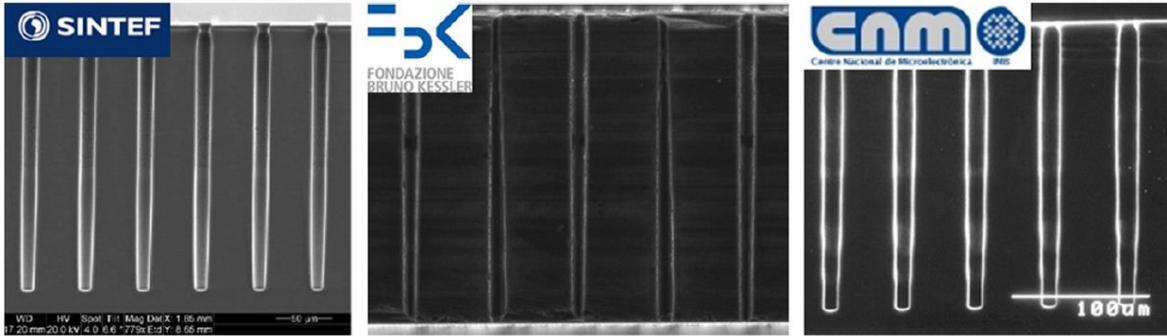
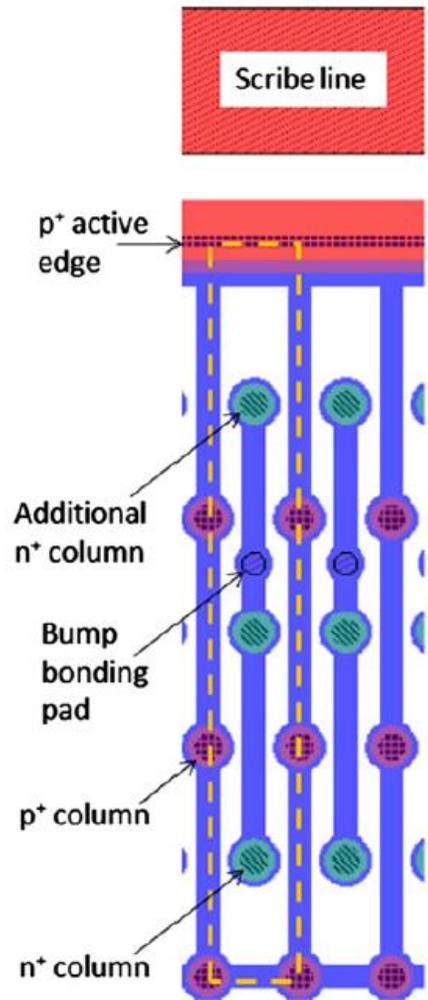
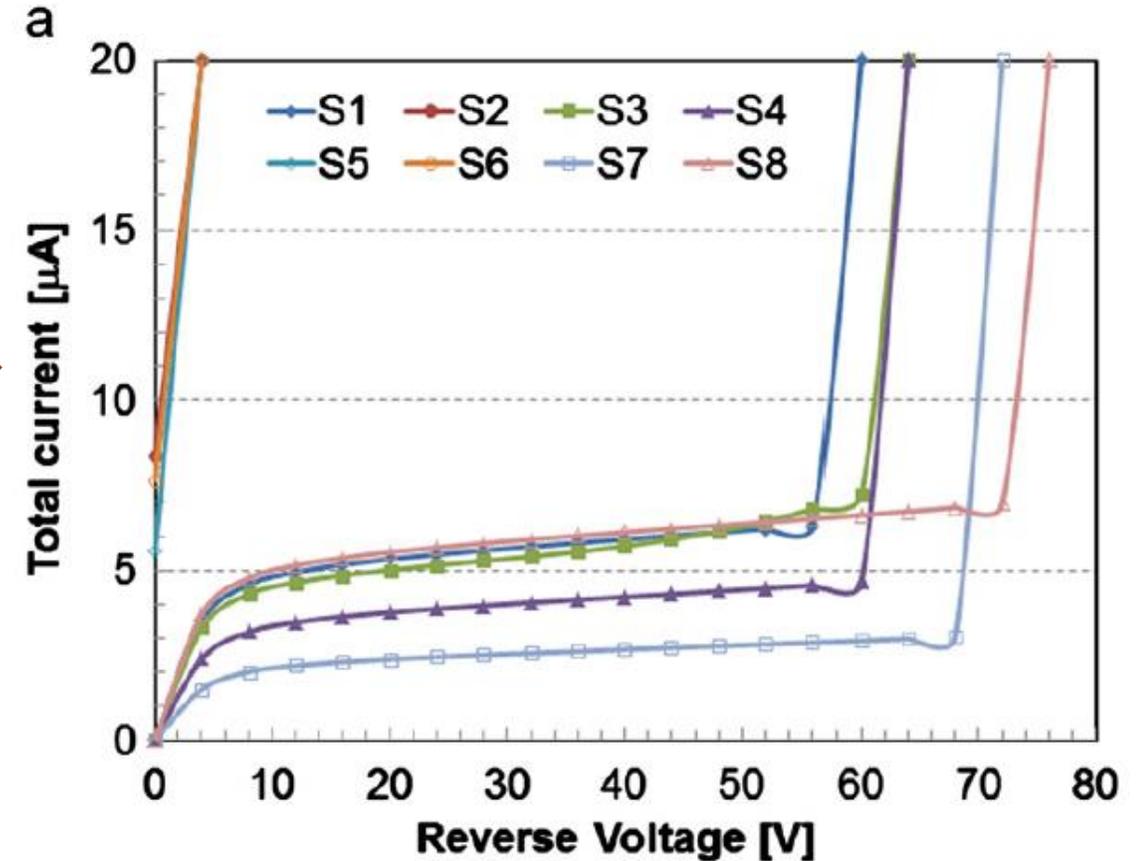


Fig. 1. Schematic cross-sections of (left) planar sensor, and (right) 3D sensor, emphasizing the decoupling of active thickness (Δ) and collection distance (L) in 3D sensors.

Acknowledgements



- Layout showing “active edge” concept for SINTEF sensor
- 8 sensors from SINTEF (from the same wafer) showing full depletion at (or below) 10 V. Three sensors show breakdown at very low voltages and would not be used in an actual experiment.



Double sided 3D

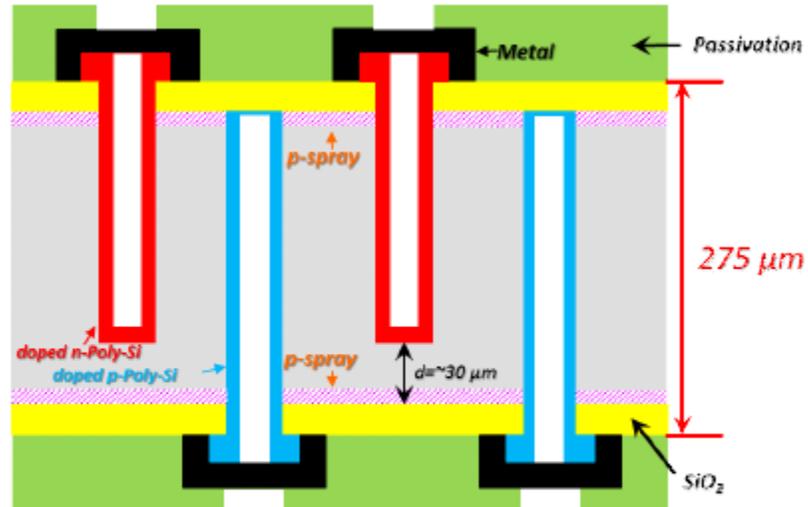
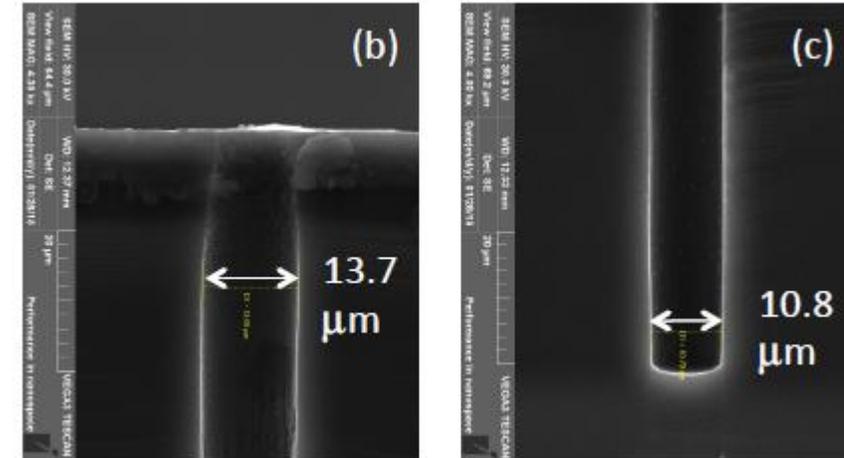


Figure 1. Schematic cross-section of the modified double-sided 3D sensors.



Column diameter at top (b) and bottom (c) of etched n-type column

Double sided 3D strip

I-V characteristic of all strips on a number of sensors from the same wafer.

